LISTING OF THE CLAIMS

1. (Original) A method for executing instructions of a computer program in a computing arrangement that includes an instruction processing engine coupled to a programmable logic device (PLD), comprising the steps of:

profiling the computer program during execution on the instruction processing engine, whereby profile data are generated for code segments in the computer program;

selecting a code segment for transformation to a hardware implementation as a function of the profile data;

transforming the code segment into a configuration bitstream that implements functionality performed by the code segment;

configuring the PLD with the configuration bitstream; and

activating the PLD in lieu of execution of the code segment during execution of the computer program.

2. (Original) The method of claim 1, wherein the profile data include execution frequencies of code segments and execution times of code segments.

3. (Original) The method of claim 1, further comprising evaluating code segments as a function of respective execution times of software implementations and execution times of hardware implementations.

4. (Original) The method of claim 1, further comprising:

implementing functions of multiple selected code segments in the PLD;

repeatedly evaluating code segments during execution of the application program as a function of the profile data;

selecting a replacement code segment as a function of the profile data for a target code segment implemented in the PLD and transforming the replacement code segment into a configuration bitstream that implements the replacement code segment in place of the target code segment; and

reconfiguring the PLD with the configuration bitstream.

5. (Original) The method of claim 4, further comprising caching configuration bitstreams associated with one or more target code segments.

6. (Original) The method of claim 4, wherein the profile data include execution frequencies of code segments and execution times of code segments.

7. (Original) The method of claim 4, further comprising evaluating code segments as a function of respective execution times of software implementations and execution times of hardware implementations.

8. (Original) The method of claim 4, further comprising:

generating a driver code segment for interfacing with the PLD while the PLD is performing the functionality of the code segment; and

executing the driver code segment on the instruction processing engine in lieu of the code segment.

9. (Original) The method of claim 1, further comprising:

generating a driver code segment for interfacing with the PLD while the PLD is performing the functionality of the code segment; and

executing the driver code segment on the instruction processing engine in lieu of the code segment.

10. (Original) The method of claim 9, further comprising replacing the first instruction of the code segment with a branch instruction that has a target address referencing the driver code segment.

11. (Original) The method of claim 1, further comprising:

translating instructions of the computer program from a first instruction set to instructions of a second instruction set, wherein the first instruction set is associated with a processor architecture that is different from the instruction processing engine;

and

executing the instructions of the second instruction set by the instruction processing engine.

12. (Original) An apparatus for executing instructions of a computer program in a computing arrangement that includes an instruction processing engine coupled to a programmable logic device (PLD), comprising:

means for profiling the computer program during execution on the instruction processing engine, whereby profile data are generated for code segments in the computer program;

means for selecting a code segment for transformation to a hardware implementation as a function of the profile data;

means for transforming the code segment into a configuration bitstream that implements functionality performed by the code segment;

means for configuring the PLD with the configuration bitstream; and

means for activating the PLD in lieu of execution of the code segment during execution of the computer program.

13. (Original) A computing arrangement, comprising:

a bus;

an instruction processing engine coupled to the bus, the instruction processing engine configured to execute instructions selected from a first set of instructions;

a programmable logic device (PLD) coupled to the bus, the PLD having configuration ports coupled to the instruction processing engine and one or more data input/output ports; and

a memory arrangement coupled to the bus, the memory arrangement configured with an application program and a transformation program that are both executable by the instruction processing engine, the transformation program including instructions that when executed cause the instruction processing engine to profile the application program during execution and generate profile data associated with segments of code in the application program, select a code segment for

transformation to a hardware implementation as a function of the profile data, transforming the code segment into a configuration bitstream that implements functionality performed by the code segment, configure the PLD with the configuration bitstream, and activate the PLD in lieu of execution of the code segment during execution of the application program.